Abstract of the Disclosure

An improved source/drain junction configuration in a metal-oxide semiconductor transistor is provided, as well as a novel method for fabricating this junction. This configuration employs gate double sidewall spacers in the peripheral region and gate single sidewall spacers in the cell array region. The double sidewall spacers are advantageously formed to suppress the short channel effect, to prevent current leakage, and to reduce sheet resistance. The insulating layer used to form the second spacers in the peripheral region remains in the cell array region and serves as an etching stopper during the etching step of interlayer insulating layer for contact opening formation and also serves as a barrier layer during the step of silicidation formation. As a result the fabrication process of the resulting device is simplified.